HTM-OLED2.23-SPI

产品名称（**Product name**） : OLED LCM

型　　号（**Model**） : HTM-OLED2.23-SPI

编　　号（**Part number**） :

日　　期（**Date**） : 2023-07-18

深圳市鑫洪泰电子科技有限公司 **Shenzhen Hot Display Technology Co.,Ltd**		
编制 **Prepared by**	审核 **Checked by**	核准 **Approved by**

编码：QR-R-011　A/0　　序号：

Rev.	Descriptions	Date
01	Prelimiay Release	2023-07-18

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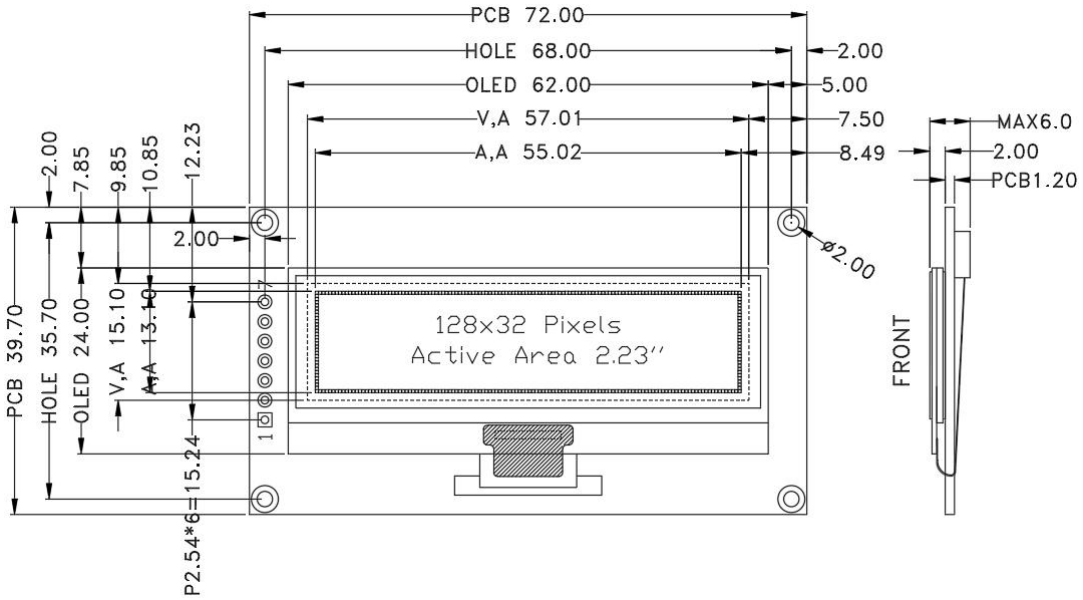
1. Bsaic Specifications

1.1 Display Specifications

1>LCD Display Mode : OLED DISPLAY Passive Matrix
2>Driving Duty : 1/64
3>Driving IC : SSD1305
4>Display Color : Monochrome (WHITE)
5>Interface : 4line-SPI

1.2 Mechanical Specifications

1>Outline Dimension

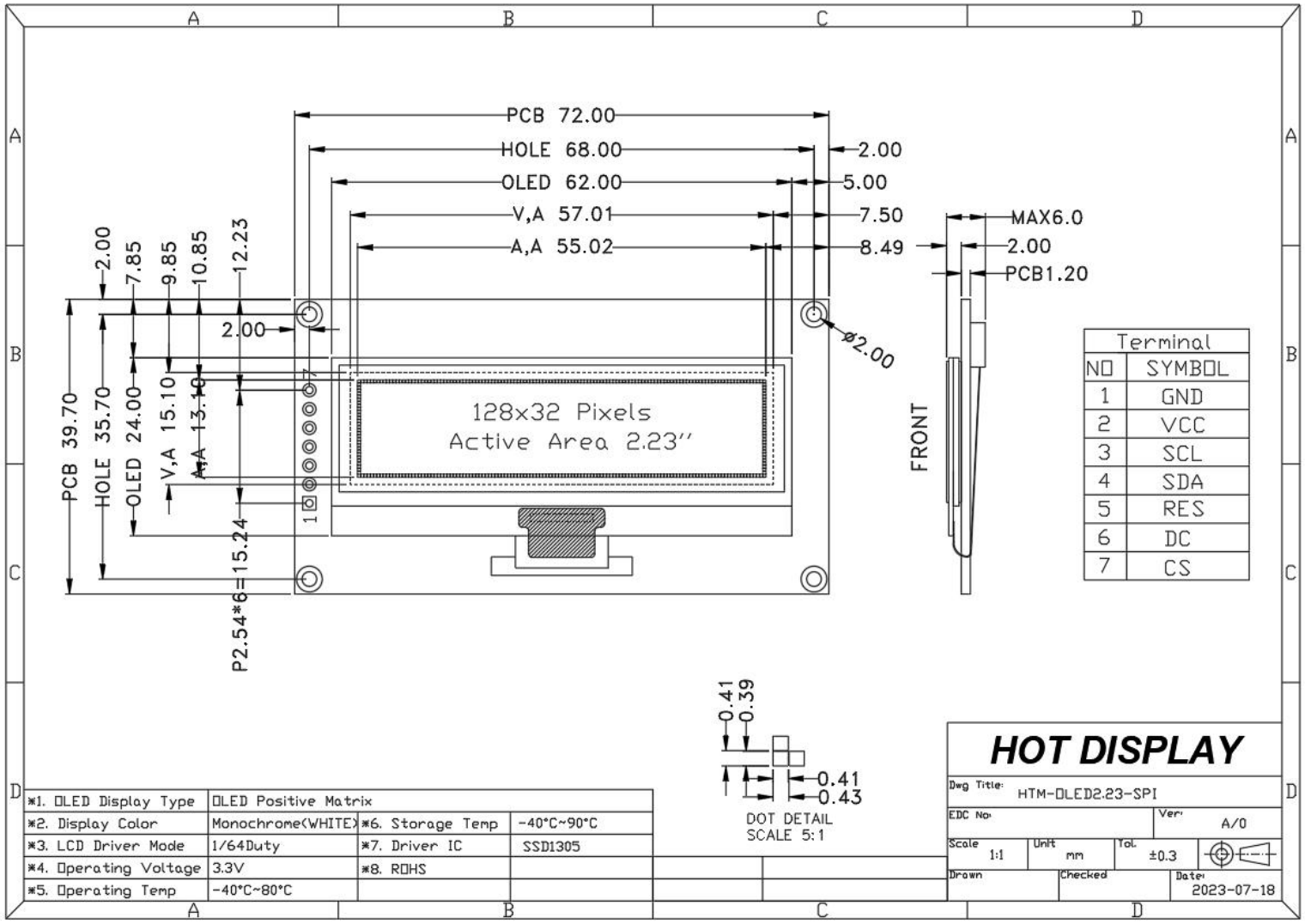


NO.	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128(W)×32(H)	-
2	Dot Size	0.41(W)×0.39 (H)	mm
3	Dot Pitch	0.43(W)×0.41 (H)	mm
4	Active Area	55.02(W)×13.10 (H)	mm
5	Module Size	72.0(W)×39.7(H)×6.0 (T)	mm
6	Diagonal A/A Size	2.23	inch
7	Module Weight	13±10%	gram

1.3 Terminal Function

Pin No.	Pin Name	Function
1	GND	Negative power supply,0V
2	VCC	Power supply voltage (Positive)
3	SCL	The serial clock input (SCL)
4	SDA	Serial data input (SDA)
5	RES	Reset Pin
6	DC	Data/Command Control
7	CS	This is the chip select signal.

1.4 Product Outline



2. Absolute Maximum Ratings

Items	Symbol	MIN.	MAX.	Unit
Supply Voltage	VBAT	3.0	4.0	V
Logic Signal Voltage	VDDIO	2.5	3.3	V
Driver Supply Voltage	VCC	0	15	V
Vcc Supply Current	ICC		55	mA
Operating Temperature	TOP	-40	+80	℃
Storage Temperature	Tst	-40	+90	℃
Humidity	RH		90%(MAX60℃)	

3. Electrical Characteristics

3.1 DC Characteristics

Vss = 0V,Top = 25℃

Items	Symbol	MIN.	TYP.	MAX.	Unit
Power Supply Voltage	VBAT	2.8	3.3	3.5	V
Logic Signal Voltage	VIH	2.8	-	3.3	
Output High Voltage	VOH	0.8 x VDDIO	-	VDDIO	V
Output Low Voltage	VOL	0	-	0.2 x VDDIO	V
Logic Current	IVBAT	-	200	-	mA
Display Voltage	VCC	11.5	12.0	12.5	V
Brightness(Yellow)	Lbr	60	90	-	Cd/m²
Dark Room Contrast	CR		＞2000:1		
View Angle			Full View		Degree

Note1: This is a voltage supply pin. It must be connected to external source

Note2: From to internally DC/DC Circuit. No need external supply.

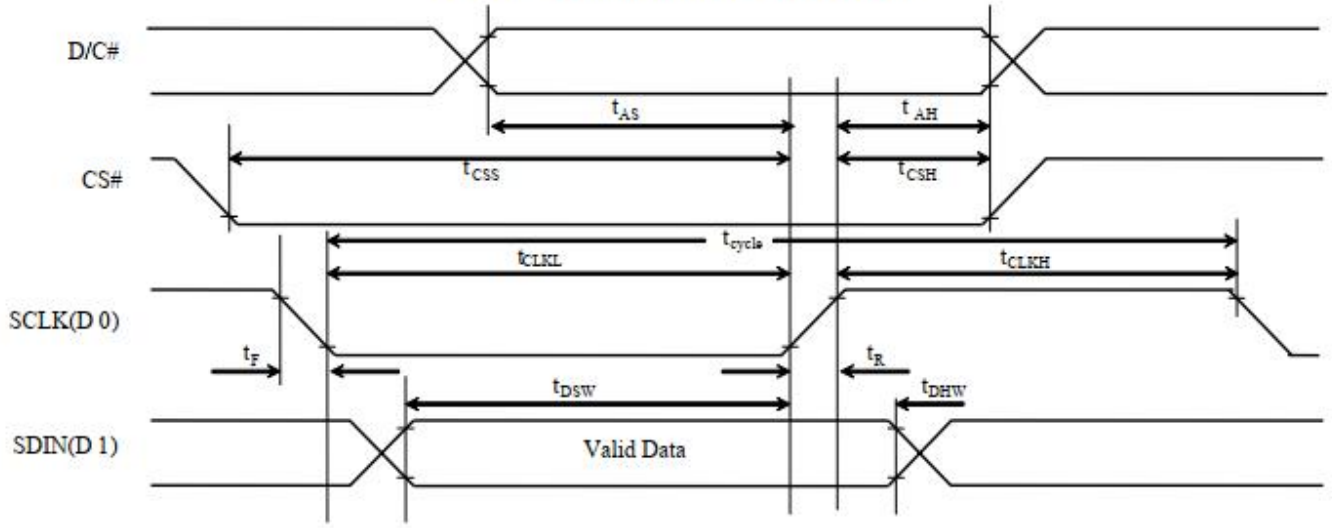
Note3: VDD=3.3V, VCC=12.0V (VDD, VCC Supply by the module internal generate) 100% Display Area Turn on.

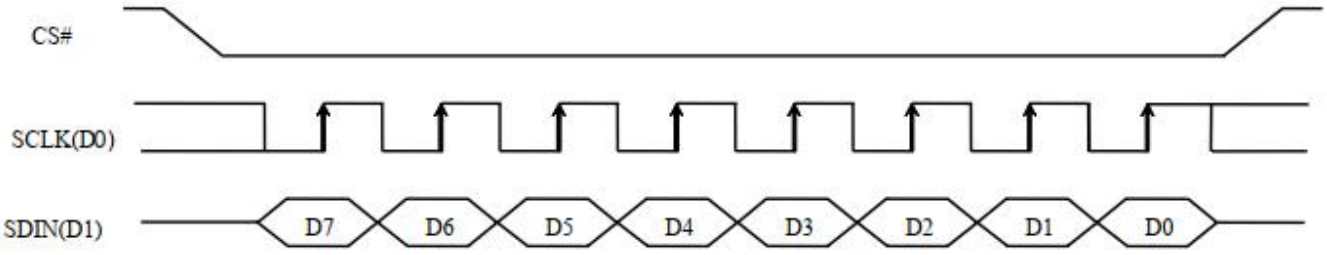
3.2 4-line SPI Mode

(V_{DD} - V_{SS} = 2.4V to 3.5V , V_{DDIO} = V_{DD} ,T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	50	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

Figure 13-4 : Serial interface characteristics





4. Function specifications

4.1 Display Commands

(D/C#=0, R/W#(WR#) = 0, E(RD#=1) unless specific setting is stated)

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00~0F	0	0	0	0	X_3	X_2	X_1	X_0	Set Lower Column Start Address for Page Addressing Mode	Set the lower nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET.
0	10~1F	0	0	0	1	X_3	X_2	X_1	X_0	Set Higher Column Start Address for Page Addressing Mode	Set the higher nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET.
0 0	20 A[1:0]	0 *	0 *	1 *	0 *	0 *	0 *	0 A_1	0 A_0	Set Memory Addressing Mode	A[1:0] = 00b, Horizontal Addressing Mode A[1:0] = 01b, Vertical Addressing Mode A[1:0] = 10b, Page Addressing Mode (RESET) A[1:0] = 11b, Invalid
0 0 0	21 A[7:0] B[7:0]	0 A_7 B_7	0 A_6 B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Setup column start and end address A[7:0] : Column start address, range : 0-131d, (RESET=0d) B[7:0]: Column end address, range : 0-131d, (RESET =131d)
0 0 0	22 A[2:0] B[2:0]	0 * *	0 * *	1 * *	0 * *	0 * *	0 A_2 B_2	1 A_1 B_1	0 A_0 B_0	Set Page Address	Setup page start and end address A[2:0] : Page start Address, range : 0-7d, (RESET = 0d) B[2:0] : Page end Address, range : 0-7d, (RESET = 7d)
0	40~7F	0	1	X_5	X_4	X_3	X_2	X_1	X_0	Set Display Start Line	Set display RAM display start line register from 0-63 using $X_5X_4X_3X_2X_1X_0$. Display start line register is reset to 000000b during RESET.
0 0	81 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Contrast Control For BANK0	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (RESET = 80h)
0 0	82 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Brightness For Area Color Banks	Double byte command to select 1 out of 256 brightness steps. Brightness increases as the value increases. (RESET = 80h)
0 0 0 0 0	91 X[5:0] A[5:0] B[5:0] C[5:0]	1 * * * *	0 * * * *	0 X_5 A_5 B_5 C_5	1 X_4 A_4 B_4 C_4	0 X_3 A_3 B_3 C_3	0 X_2 A_2 B_2 C_2	0 X_1 A_1 B_1 C_1	1 X_0 A_0 B_0 C_0	Set Look Up Table (LUT)	Set current drive pulse width of BANK0, Color A, B and C. BANK0: X[5:0] = 31… 63; for pulse width set to 32 ~ 64 clocks (RESET = 110001b) Color A: A[5:0] same as above (RESET = 111111b) Color B: B[5:0] same as above (RESET = 111111b) Color C: C[5:0] same as above (RESET = 111111b) **Note** (1) Color D pulse width is fixed at 64 clocks pulse.

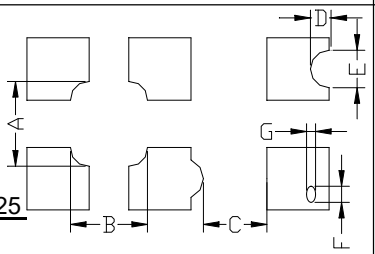
Fundamental Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0 0 0 0	92 A[7:0] B[7:0] C[7:0] D[7:0]	1 A_7 B_7 C_7 D_7	0 A_6 B_6 C_6 D_6	0 A_5 B_5 C_5 D_5	1 A_4 B_4 C_4 D_4	0 A_3 B_3 C_3 D_3	0 A_2 B_2 C_2 D_2	1 A_1 B_1 C_1 D_1	0 A_0 B_0 C_0 D_0	Set Bank Color of BANK1 to BANK16 (PAGE0)	Set the bank color of BANK1~BANK16 to any one of the 4 colors : A, B, C and D . A[1:0] : 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK1 A[3:2] : 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK2 : : D[5:4]: 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK15 D[7:6]: 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK16
0 0 0 0 0	93 A[7:0] B[7:0] C[7:0] D[7:0]	1 A_7 B_7 C_7 D_7	0 A_6 B_6 C_6 D_6	0 A_5 B_5 C_5 D_5	1 A_4 B_4 C_4 D_4	0 A_3 B_3 C_3 D_3	0 A_2 B_2 C_2 D_2	1 A_1 B_1 C_1 D_1	1 A_0 B_0 C_0 D_0	Set Bank Color of BANK17~BANK32 (PAGE1)	Set the bank color of BANK17~BANK32 to any one of the 4 colors: A, B, C and D. A[1:0] : 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK17 A[3:2] : 00b, 01b, 10b, or 1b1 for Color = A, B, C or D of BANK18 : : D[5:4]: 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK31 D[7:6]: 00b, 01b, 10b, or 11b for Color = A, B, C or D of BANK32
0	A0/A1	1	0	1	0	0	0	0	X_0	Set Segment Re-map	X[0]=0b: column address 0 is mapped to SEG0 (RESET) X[0]=1b: column address 131 is mapped to SEG0
0	A4/A5	1	0	1	0	0	1	0	X_0	Entire Display ON	X_0=0b: Resume to RAM content display (RESET) Output follows RAM content X_0=1b: Entire display ON Output ignores RAM content
0	A6/A7	1	0	1	0	0	1	1	X_0	Set Normal/Inverse Display	X[0]=0b: Normal display (RESET) 0 in RAM: OFF in display panel 1 in RAM: ON in display panel X[0]=1b: inverse display 0 in RAM: ON in display panel 1 in RAM: OFF in display panel
0 0	A8 A[5:0]	1 *	0 *	1 A_5	0 A_4	1 A_3	0 A_2	0 A_1	0 A_0	Set Multiplex Ratio	Set MUX ratio to N+1 MUX N=A[5:0] : from 16MUX to 64MUX, RESET= 111111b (i.e. 64MUX) A[5:0] from 0 to 14 are invalid entry.
0	AA	1	0	1	0	1	0	1	0	Reserved	Reserved
0 0 0 0	AB A[3:0] B[7:0] C[7:0]	1 * B_7 C_7	0 * B_6 C_6	1 * B_5 C_5	0 * B_4 C_4	1 A_3 B_3 C_3	0 A_2 B_2 C_2	1 A_1 B_1 C_1	1 A_0 B_0 C_0	Dim mode setting	A[3:0] : Reserved (set as 0000b) B [7:0] : Set contrast for BANK0, valid range 0-255d, please refer to command 81h C [7:0] : Set brightness for color bank, valid range 0-255d, please refer to command 82h

Fundamental Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	AD A[7:0]	1 1	0 0	1 0	0 0	1 1	1 1	0 1	1 A_0	Master Configuration	A[0]=0b, Select external V_{CC} supply (RESET) A[0]=1b, Select internal DC-DC voltage converter Note (1) Refer to Section 8.11 for DC-DC converter details (2) The DC-DC converter must be enabled by the following command: ADh ; Master Configuration 8Fh ; Enable internal DC-DC AFh or ACh ; Display ON
0	AC AE AF	1	0	1	0	1	1	A_1	A_0	Set Display ON/OFF	ACh = Display ON in dim mode AEh = Display OFF (sleep mode) (RESET) AFh = Display ON in normal mode
0	B0~B7	1	0	1	1	0	X_2	X_1	X_0	Set Page Start Address for Page Addressing Mode	Set GDDRAM Page Start Address (PAGE0~PAGE7) for Page Addressing Mode using X[2:0].
0	C0/C8	1	1	0	0	X_3	0	0	0	Set COM Output Scan Direction	X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N –1] X[3]=1b: remapped mode. Scan from COM[N~1] to COM0 Where N is the Multiplex ratio.
0 0	D3 A[5:0]	1 *	1 *	0 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Display Offset	Set vertical shift by COM from 0~63. The value is reset to 00h after RESET.
0	D5 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	0 A_3	1 A_2	0 A_1	1 A_0	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0] : Define the divide ratio (D) of the display clocks (DCLK): Divide ratio= A[3:0] + 1, RESET is 0000b (divide ratio = 1) A[7:4] : Set the Oscillator Frequency, F_{OSC}. Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 0111b Range:0000b~1111b Frequency increases as setting value increases. Refer to section 10.1.23 for details.
0 0	D8	1 0	1 0	0 X_5	1 X_4	1 0	0 X_2	0 0	0 X_0	Set Area Color Mode ON/OFF & Low Power Display Mode	X[5:4]= 00b (RESET) : monochrome mode X[5:4]= 11b Area Color enable X[2]=0b and X[0]=0b: Normal power mode(RESET) X[2]=1b and X[0]=1b: Set low power display mode
0 0	D9 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	1 A_3	0 A_2	0 A_1	1 A_0	Set Pre-charge Period	A[3:0] : Phase 1 period of up to 15 DCLK clocks (RESET=2h); 0 is invalid entry A[7:4] : Phase 2 period of up to 15 DCLK clocks (RESET=2h); 0 is invalid entry

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	DA	1 0	1 0	0 X_5	1 X_4	1 0	0 0	1 1	0 0	Set COM Pins Hardware Configuration	X[4]=0b, Sequential COM pin configuration X[4]=1b(RESET), Alternative COM pin configuration X[5]=0b(RESET), Disable COM Left/Right remap X[5]=1b, Enable COM Left/Right remap Please refer to Table 10-3 for details.
0 0	DB A[5:2]	1 0	1 0	0 A_5	1 A_4	1 A_3	0 A_2	1 0	1 0	Set V_{COMH} Deselect Level	<table><tr><th>A[5:2]</th><th>Hex code</th><th>V_{COMH} deselect level</th></tr><tr><td>0000b</td><td>00h</td><td>~ 0.43 x V_{CC}</td></tr><tr><td>1101b</td><td>34h</td><td>~ 0.77 x V_{CC} (RESET)</td></tr><tr><td>1111b</td><td>3Ch</td><td>~ 0.83 x V_{CC}</td></tr></table>
0	E0	1	1	1	0	0	0	0	0	Enter Read Modify Write	Enter the Read Modify Write mode. Details please refer to section 10.1.28.
0	E3	1	1	1	0	0	0	1	1	NOP	Command for no operation
0	EE	1	1	1	0	1	1	1	0	Exit Read Modify Write	Exit the Read Modify Write mode (Please refer to command E0h)

5. Inspection Standards

Item	Criterion for defects	Defect type
1) Display on inspection	(1) Non display (2) Vertical line is deficient (3) Horizontal line is deficient (4) Cross line is deficient	Major
2) Black / White spot	Size Φ(mm) Acceptable number Φ≤0.3 Ignore (note) 0.3<Φ≤0.45 3 0.45<Φ≤0.6 1 0.6<Φ 0	Minor
3) Black / White line	Length (mm) Width (mm) Acceptable number L≤10 W≤0.03 Ignore 5.0≤L≤10 0.03<W≤0.04 3 5.0≤L≤10 0.04<W≤0.05 2 1.0≤L≤10 0.05<W≤0.06 2 1.0≤L≤10 0.06<W≤0.08 1 L≤10 0.08<W follows 2) point defect Defects separate with each other at an interval of more than 20mm	Minor
4) Display pattern	 $\frac{A+B}{2}\leq 0.28$ | $0<C$ | $\frac{D+E}{2}\leq 0.25$ | $\frac{F+G}{2}\leq 0.25$ Note: 1) Up to 3 damages acceptable 2) Not allowed if there are two or more pinholes every three-fourth inch.	Minor
5) Spot-like contrast irregularity	Size Φ(mm) Acceptable Number Φ≤0.7 Ignore (note) 0.7<Φ≤1.0 3 1.0<Φ≤1.5 1 1.5<Φ 0 Note: 1) Conformed to limit samples. 2) Intervals of defects are more than 30mm.	Minor
6) Bubbles in polarizer	Size Φ(mm) Acceptable Number Φ≤0.4 Ignore (note) 0.4<Φ≤0.65 2 0.65<Φ≤1.2 1 1.2<Φ 0	Minor
7) Scratches and dent on the polarizer	Scratches and dent on the polarizer shall be in the accordance with “2) Black/white spot”, and “3) Black/White line”.	Minor
8) Stains on the surface of LCD panel	Stains which cannot be removed even when wiped lightly with a soft cloth or similar cleaning.	Minor
9) Rainbow color	No rainbow color is allowed in the optimum contrast on state within the active area.	Minor
10) Viewing area encroachment	Polarizer edge or line is visible in the opening viewing area due to polarizer shortness or sealing line.	Minor
11) Bezel appearance	Rust and deep damages that are visible in the bezel are rejected.	Minor
12) Defect of land surface contact	Evident crevices that are visible are rejected.	Minor
13) Parts mounting	(1) Failure to mount parts (2) Parts not in the specifications are mounted (3) For example: Polarity is reversed, HSC or TCP falls off.	Minor
14) Part alignment	(1) LSI, IC lead width is more than 50% beyond pad outline. (2) More than 50% of LSI, IC leads is off the pad outline.	Minor
15) Conductive foreign matter (solder ball, solder hips)	(1) 0.45<Φ, N≥1 (2) 0.3<Φ≤0.45, N≥1, Φ: Average diameter of solder ball (unit: mm) (3) 0.5<L, N≥1, L: Average length of solder chip (unit: mm)	Minor
16) Bezel flaw	Bezel claw missing or not bent	Minor
17) Indication on name plate (sampling indication label)	(1) Failure to stamp or label error, or not legible.(all acceptable if legible) (2) The separation is more than 1/3 for indication discoloration, in which the characters can be checked.	Minor

6. Handling Precautions

6.1 Mounting method

A panel of LCD module made by our company consists of two thin glass plates with polarizers that easily get damaged.

And since the module in so constructed as to be fixed by utilizing fitting holes in the printed circuit board (PCB), extreme care should be used when handling the LCD modules.

6.2 Cautions of LCD handling and cleaning

When cleaning the display surface, use soft cloth with solvent (recommended below) and wipe lightly.

-Isopropyl alcohol

-Ethyl alcohol

-Trichlorotriflorothane

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

-Water

-Ketene

-Aromatics

6.3 Caution against static charge

The LCD module use C-MOS LSI drivers. So we recommend you:

Connect any unused input terminal to V_{dd} or V_{ss}. Do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

6.4 Packaging

-Module employs LCD elements, and must be treated as such. Avoid intense shock and falls from a height.

-To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity.

6.5 Caution for operation

-It is an indispensable condition to drive LCD module within the limits of the specified voltage since the higher voltage over the limits may cause the shorter life of LCD module.

-An electrochemical reaction due to DC (direct current) causes LCD undesirable deterioration so that the uses of DC (direct current) drive should be avoided.

-Response time will be extremely delayed at lower temperature than the operating temperature range and on the other hand at higher temperature LCD module may show dark color in them. However those phenomena do not mean malfunction or out of order of LCD module, which will come back in the specified operating temperature.

6.6 Storage

In the case of storing for a long period of time, the following ways are recommended:

-Storage in polyethylene bag with the opening sealed so as not to enter fresh air outside in it. And with not desiccant.

-Placing in a dark place where neither exposure to direct sunlight nor light is. Keeping the storage temperature range.

-Storing with no touch on polarizer surface by any thing else.

6.7 Safety

-It is recommendable to crash damaged or unnecessary LCD into pieces and to wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.

-When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well at once with soap and water.